CLAIMS

What is claimed is:

1. In a multiprocessor computer system having a plurality of processing nodes coupled in an array wherein each processing node is coupled to at least one other processing node, and a memory distributed among the plurality of processing nodes, a method of testing the memory comprising the steps of:

determining a configuration of the array;

determining an initial configuration of the memory;

testing the memory over the array according to said initial configuration to identify a bad memory element; and

modifying said initial configuration to form a revised configuration that excludes said bad memory element.

2. The method of claim 1 further comprising the step of:

passing control of the multiprocessor computer system with said revised configuration to an operating system.

3. The method of claim 1 wherein said step of modifying said initial configuration to form said revised configuration comprises the steps of:

identifying a bad memory block corresponding to said bad memory element; and

forming said revised configuration to exclude said bad memory block.

4. The method of claim 3 wherein said step of modifying comprises the steps of:

determining a node and a chip select on said node with which said bad memory block is associated using said physical address; and

reconfiguring the memory by disabling said chip select on said node.

5. The method of claim 1 further comprising the steps of:

identifying one of the plurality of processing nodes that is to be a boot strap processor;

performing said step of testing using said boot strap processor.

6. The method of claim 1 wherein said step of modifying said initial configuration to form said revised configuration comprises the step of:

communicating said revised configuration to each of the plurality of processing nodes.

7. The method of claim 1 wherein said step of determining said initial configuration comprises the step of:

communicating said initial configuration to each of the plurality of processing nodes before said step of testing.

8. The method of claim 1 wherein said step of determining said initial configuration comprises the step of determining said initial configuration using a system management bus coupled to the memory.

9. In a multiprocessor computer system having a plurality of processing nodes and a memory distributed among the plurality of processing nodes, a method of testing the memory comprising the steps of:

configuring the memory by programming the plurality of processing nodes with an initial configuration;

testing the memory using said initial configuration to identify a bad memory element;

determining a node and a region defined on said node which are associated with said bad memory element;

reconfiguring the memory by programming the plurality of processing nodes with a revised configuration that excludes said region; and

operating the multiprocessor computer system using said revised configuration.

10. The method of claim 9 wherein said step of operating comprises the step of:

passing control of the multiprocessor computer system with said revised configuration to an operating system.

11. The method of claim 9 wherein said step of determining said node and said region comprises the steps of, for successive ones of the plurality of processing nodes and until said region is found:

determining a last enabled region on a respective processing node, if any; and

determining whether a physical address of said bad memory element falls within said last enabled region.

12. The method of claim 9 further comprising the step of:

determining said initial configuration prior to said step of configuring the memory.

13. The method of claim 12 wherein said step of determining said initial configuration comprises the step of determining said initial configuration using a system management bus coupled to the memory.

14. The method of claim 9 further comprising the steps of:

identifying one of the plurality of processing nodes that is to be a boot strap processor;

performing said steps of configuring, testing, determining, and reconfiguring using said boot strap processor.

15. The method of claim 14 wherein said step of identifying comprises the step of determining that a communication controller of said one of the plurality of processing nodes is connected to a Southbridge.

16. For use in a multiprocessor computer system including:

a plurality of processing nodes coupled in an array wherein each processing node is coupled to at least one other processing node; and

a memory distributed among the plurality of processing nodes,

a basic input/output system (BIOS) memory adapted to be coupled to one of the plurality of processing nodes, designated a boot strap processor (BSP), said BIOS memory comprising:

a first set of instructions executable by said BSP to determine a configuration of the array;

a second set of instructions executable by said BSP to determine an initial configuration of the memory;

a third set of instructions executable by said BSP to test the memory over the array according to said initial configuration to identify a bad memory element; and

a fourth set of instructions executable by said BSP to modify said initial configuration to form a revised configuration that excludes said bad memory element.

17. The BIOS memory of claim 16 wherein said first, second, third, and fourth sets of instructions are stored in a mask read only memory (ROM).

18. The BIOS memory of claim 16 wherein said first, second, third, and fourth sets of instructions are stored in an erasable programmable read only memory (EPROM).

19. The BIOS memory of claim 16 further comprising a fifth set of instructions executable by said BSP for passing control of the multiprocessor computer system with said revised configuration to an operating system.

20. The BIOS memory of claim 16 wherein said fourth set of instructions provides information about said bad memory element to said first set of instructions and causes said first set of instructions to be re-executed.

21. The BIOS memory of claim 16 wherein said second set of instructions further causes said boot strap processor to communicate said initial configuration to said plurality of processing nodes over the array.

22. For use in a multiprocessor computer system including:

a plurality of processing nodes coupled in an array wherein each processing node is coupled to at least one other processing node; and

a memory distributed among the plurality of processing nodes,

a basic input/output system (BIOS) memory adapted to be coupled to one of the plurality of processing nodes, designated a boot strap processor (BSP), said BIOS memory comprising:

a first set of instructions executable by said BSP to configure the memory by programming the plurality of processing nodes with an initial configuration;

a second set of instructions executable by said BSP to test the memory using said initial configuration to identify a bad memory element;

a third set of instructions executable by said BSP to determine a node and a region defined on said node which are associated with said bad memory element;

a fourth set of instructions executable by said BSP to reconfigure the memory by programming the plurality of processing nodes with a revised configuration that excludes said region; and

a fifth set of instructions executable by said BSP to operate the multiprocessor computer system using said revised configuration.

23. The BIOS memory of claim 22 wherein said first, second, third, fourth, and fifth sets of instructions are stored in a mask read only memory (ROM).

24. The BIOS memory of claim 23 wherein said first, second, third, fourth, and fifth sets of instructions are stored in an erasable programmable read only memory (EPROM).

25. The BIOS memory of claim 22 wherein said fifth set of instructions operates the multiprocessor computer system using said revised configuration by transferring control to an operating system.

26. The BIOS memory of claim 22 wherein said fourth set of instructions provides information about said bad memory element to said first set of instructions and causes said first set of instructions to be re-executed.

27. The BIOS memory of claim 22 wherein said second set of instructions further causes said boot strap processor to communicate said initial configuration to said plurality of processing nodes over the array.